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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,226	11/25/2003	Jean Audet	END920030089us1	6701

7590 05/02/2006

John A. Jordan
11 Hyspot Road
Greenfield Center, NY 12833

EXAMINER	
SEMENENKO, YURIY	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 05/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/722,226	AUDET ET AL.	
	Examiner	Art Unit	
	Yuriy Semenenko	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *03 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *10-18 and 22-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 19-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Amendments filed on 02/03/2006 have been entered. In response to the Office Action dated 01/09/2006, Applicants has amended claims 1 and 19. Claims 10-18 and 22-30 had been withdrawn from consideration.
Claims 1-30 are now pending in the application.

Claim Objections

2. Applicant's assent to eliminate discrepancy of the claims 11-18 accordingly with examiner's objection is acknowledged.

Election/Restrictions

3. Applicant's election with traverse of claims 1-9 and 19-21 in the reply filed on 02/03/2006 is acknowledged.
Though applicant's arguments are somewhat persuasive, there are another reasons to restrict the claims between the groups. Claims of group II need the steps of moving a set of signal pads. The product does not need such steps. The product can be made with a predetermined design locations.

The requirement is still deemed proper and is therefore made FINAL.

Specification

4. The Specification amendments, filed on 02/03/2006 accordingly with examiner's objection is acknowledged and approved.

Claim Objections

5. The claim 1 amendment filed on 02/03/2006 accordingly with examiner's objection is acknowledged and approved.

Response to Arguments

6. Applicant's arguments filed 02/03/2006 have been considered but are moot in view of the new grounds of rejection.

Drawings

7. Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

8. Claim 19 is objected to for improper antecedent. Claim 19 recites the limitation "the footprint" should be "a footprint". There is insufficient antecedent basis for this limitation.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9.1. Claims 19-21 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As to claims 19: It is unclear what kind of signal pads positioned closer to the edge of said chip footprint mean as respective pads and what kind of pads having conductive vias in such sentence "a second set of signal pads each having a conductive line connected thereto extending to connect to respective signal pads positioned closer to the edge of said chip footprint with said signal pads positioned closer to the edge of said chip footprint having conductive vias connected thereto extending through said first layer of dielectric material;"

To apply art, Examiner assumed that -- a second set of signal pads each having a conductive line connected thereto extending to connect to respective signal pads of the first set of signal pads positioned closer to the edge of said chip footprint with the signal pads of the second set of signal pads having conductive vias connected thereto extending through said first layer of dielectric material; --

Claims 20 and 21 depend on claim 19 and have same deficiency.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented

and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10.1. Claims 1-4, 8, 9 and 19-21 are rejected under 35U.S.C. 103(a) as being obvious over Admitted by Applicant (Prior Art, hereinafter "APA") in view of Buschbom (Patent # 6800944 hereafter "Buschbom") .

As to claim 1: APA discloses in Fig. 1 a multilayer chip carrier, comprising: a layer of dielectric material (dielectric layer having signal redistribution layer FC3, Fig. 4 and Specification, page 8, line 25), having a plurality of signal pads (37, Fig. 4) formed thereon in a pattern of signal pads related to a pattern of signal pads within the footprint of at least one chip (7, Fig. 1), to be carried on said chip carrier, said plurality of signal pads including a first set of signal pads near the edge of said chip footprint 37a, 37b, 37c , Fig. 4 (inside region 31) each having a conductive line 39 connected thereto extending beyond the edge 23 of said chip footprint and a second set of signal pads 37 (inside region 29, Fig. 4), having a conductive line 41 connected thereto,

except APA doesn't explicitly teach that second set of signal pads each having a conductive line connected thereto extending to connect to respective signal pads positioned nearer the said edge of said chip footprint.

Buschbom discloses in prior art drawing of Fig.2 set of signal pads 14, 46 (column 3, lines 62-67) each having a conductive line 15, 44 connected thereto extending to connect to respective signal pads 14 positioned nearer the said edge of said chip footprint. At time the invention was made, it was well know to use signal pads

each having a conductive line connected thereto extending to connect to respective signal pads positioned nearer the said edge of said chip footprint.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for APA to include in his invention that second set of signal pads each having a conductive line connected thereto extending to connect to respective signal pads positioned nearer the said edge of said chip footprint to have designed electrical connections.

As to claim 2: APA discloses in Fig. 1 the multilayer chip carrier having all of the claimed features as discussed above with respect claim 1, wherein at least some of said signal pads (37, Fig. 4) on said dielectric layer nearer the said edge of said chip footprint have a conductive via connected thereto that form a set of conductive vias that extend through said layer of dielectric material to the opposing surface thereof (Specification, page 8, lines 24- 25 and page 9, lines 1-4).

As to claim 3: APA discloses in Fig. 1 the multilayer chip carrier having all of the claimed features as discussed above with respect claim 2, including a further layer (FC 2 Layer, Fig. 5) of dielectric material beneath said layer (FC3, Fig. 4) of dielectric material having signal pads 37 and 37A thereon (FC 2 Layer, Fig. 5), with respective ones of said signal pads connected to respective ones of said conductive vias of said set of conductive vias (Specification, page 8, lines 24- 25 and page 9, lines 1-4).

As to claim 4: APA discloses in Fig. 1 the multilayer chip carrier having all of the claimed features as discussed above with respect claim 3, wherein at least some of said signal pads on said further layer(FC 2 Layer, Fig. 5), of dielectric material each have a conductive line 41 connected thereto,

except APA doesn't explicitly teach a conductive line connected thereto extending to connect to respective further signal pads nearer the edge of said chip footprint.

Buschbom discloses in prior art drawing of Fig.2 set of signal pads 14, 46 (column 3, lines 62-67) each having a conductive line 15, 44 connected thereto extending to connect to respective signal pads 14 positioned nearer the said edge of said chip footprint. At time the invention was made, it was well know to use a conductive line connected thereto extending to connect to respective signal pads positioned nearer the said edge of said chip footprint.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for APA to include in his invention that a conductive line connected thereto extending to connect to respective further signal pads nearer the edge of said chip footprint to save material for connecting lines.
Examiner note that this structure for further layer exactly the same as claimed in claim 1 for layer of dielectric material, as discussed above with respect claim 1. And further, It has been held that a mere duplication of parts, absent new or unexpected results, is within the level of ordinary skill. In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960).

As to claim 8: APA discloses in Fig. 1 the multilayer chip carrier having all of the claimed features as discussed above with respect claim 1, including a chip 7, attached thereto, Fig. 1.

As to claim 9: APA discloses in Fig. 1 the multilayer chip carrier having all of the claimed features as discussed above with respect claim 8, wherein said multilayer chip carrier is electrically attached to a printed wiring board 17, Fig. 1.

As to claim 19: APA discloses in Fig. 1 a multilayer chip carrier, comprising: a first layer (FC3, Fig. 4) of dielectric material (Specification, page 8, line 25) having a plurality of signal pads 37 formed thereon arranged in a pattern of signal pads related to signal pads within the footprint 23 of at least one chip 7, Fig. 1 to be carried by said chip carrier, said plurality of signal pads including a first set signal pads (inside region 31, Fig. 4) near the edge of said chip footprint 37a, 37b, 37c, Fig. 4 each having conductive

lines 39 connected thereto extending beyond the edge 23 of said chip footprint and a second set of signal pads 37 (inside region 29, Fig. 4) each having a conductive line 41connected thereto and having conductive vias connected thereto extending through said first layer of dielectric material (Specification, page 8, lines 24- 25 and page 9, lines 1-4), a second layer (FC2, Fig. 5) of dielectric material having a set of signal pads 37 arranged thereon respectively connected to said conductive vias 41 extending through said first layer (FC 3, Fig. 4) (Specification, page 8, lines 24- 25 and page 9, lines 1-4)of dielectric material and having respective conductive lines 41 connected thereto, said further signal pad 37, and a third layer FC1, Fig. 6 of dielectric material having a set of signal pads 37 arranged thereon and having conductive lines 39, Fig. 6 respectively connected thereto extending beyond the edge of said chip footprint,

except APA doesn't explicitly teach a second set of signal pads having a conductive line extending to connect to respective signal pads of the first set of signal pads positioned closer to the edge of said chip footprint with the signal pads of the second set of signal pads.

Buschbom discloses in prior art drawing of Fig. 2 set of pads 14, 46 (column 3, lines 62-67) having a conductive line 15, 44 connected thereto extending to connect to respective pads 14 positioned nearer the said edge of said chip footprint. Further, Buschbom teaches such pad 14, having conductive vias connected thereto. At time the invention was made, it was well know to use pads having a conductive line connected thereto extending to connect to pads positioned nearer the edge of the chip footprint.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for APA to include in his invention that a second set of signal pads having a conductive line extending to connect to respective signal pads of the first set of signal pads positioned closer to the edge of said chip footprint with the signal pads of the second set of signal pads to decrease number of the layers of the circuit board.

Although, APA doesn't explicitly teach that a third layer of dielectric material having a set of signal pads respectively connected to the said conductive vias extending through said second layer of dielectric material. But APA explicitly discloses the conductive vias

extending through the first layer of dielectric material (see above). Buschbom also discloses conductive vias extending through the layer of dielectric material. And further, It has been held that a mere duplication of parts, absent new or unexpected results, is within the level of ordinary skill. In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960). Therefore, at time the invention was made, it was well know to use conductive vias connected to pads and extending through said second layer of dielectric material.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for APA to include in his invention the conductive vias extending through said second layer of dielectric material to provide connections between layers.

As to claim 20: APA, as modified, discloses the multilayer chip carrier having all of the claimed features as discussed above with respect claim 19, including at least one chip 7, Fig. 1 having a pattern of electrical contacts corresponding to said pattern of signal pads electrically connected thereto.

As to claim 21: APA, as modified, discloses the multilayer chip carrier having all of the claimed features as discussed above with respect claim 20, wherein said chip carrier 7, Fig. 1, is electrically attached to a printed wiring board 17.

10.2. Claims 5-7 are rejected under 35U.S.C. 103(a) as being obvious over Admitted by Applicant (Prior Art, hereinafter "APA") in view of Buschbom and in view of Arima et al. (Patent #6479758 hereinafter "Arima").

As to claim 5: APA, as modified, discloses the multilayer chip carrier having all of the claimed features as discussed above with respect claim 4, wherein at least some of said further signal pads 37, Fig. 5 have conductive vias 41 connected thereto and signal pads 37 on another layer (FC 1 Layer, Fig. 6) of dielectric material having

conductive lines 39, Fig. 6 connected thereto extending beyond the edge 23 of said chip footprint,

except APA doesn't explicitly conductive vias connected thereto that extend through said further layer of dielectric material to connect to signal pads on another layer of dielectric material .

Aruma discloses in Fig. 2 respective ones of said signal pads 4a connected to respective ones of said conductive vias 18a of said set of conductive vias. At time the invention was made, it was well know to use respective ones of said signal pads connected to respective ones of said conductive vias of said set of conductive vias.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for APA to include in his invention that respective ones of said signal pads connected to respective ones of said conductive vias of said set of conductive vias t to provide connections between layers.

As to claim 6: APA, as modified, discloses the multilayer chip carrier having all of the claimed features as discussed above with respect claim 5, wherein said plurality of signal pads 37, Fig. 4 are arranged adjacent a plurality of power distribution busses 35.

As to claim 7: APA, as modified, discloses the multilayer chip carrier having all of the claimed features as discussed above with respect claim 6, wherein power PTHs 43 are connected to said power distribution busses 35 in the region of said signal pads 37.

Relevant Art

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Cornelius et al. (Patent #6834427) Saiki et al. (PGPub #2005/0023033)

12.1. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yuriy Semenenko whose telephone number is (571) 272-6106. The examiner can normally be reached on 8:30am - 5:00pm.

12.2. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571)- 272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

12.3. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Art Unit: 2481